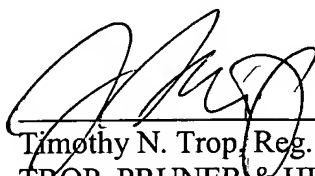## REMARKS

The cited Mason reference shows nothing whatsoever of any pertinency. In fact, Mason himself indicates that the write-back is done "as usual," or in other words, completely in keeping with the prior art. See column 10, line 40. Nothing in Mason suggests that he does two non-sequential write operations as one write operation. Mason does not even do two sequential writes as one write operation. He does look for the next write operation to be as close to the one that was just done, but this is not combining two writes into one. Mason is just an example of the typical prior art and has no relevancy whatsoever to the claimed invention.

Therefore, reconsideration is requested.

Regarding the suggestion that Mason teaches a "potentially" non-sequentially cached logical disk block, Mason's "potential" has no weight in the patentability determination. Anybody could do anything if they had only thought of it. Mason did not think of it.

Respectfully submitted,

Date: <u>August 10, 2006</u>

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation